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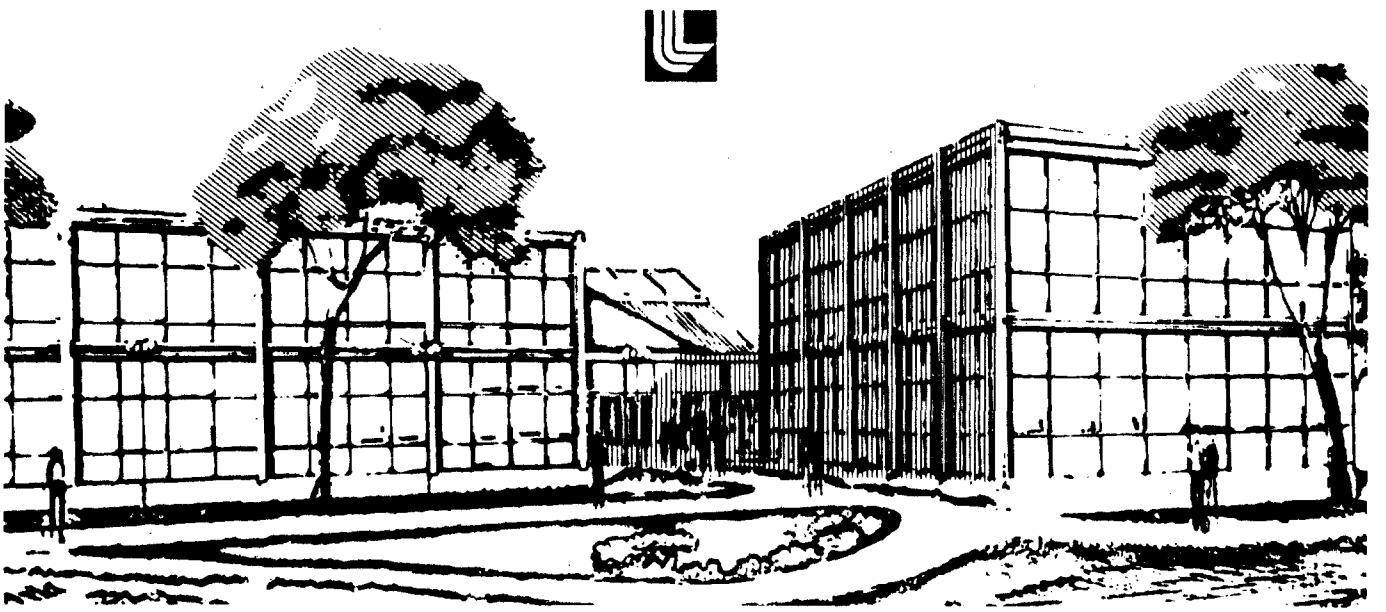

VIDEO DRIVER/EXTENDED MEMORY FOR THE LSI-11*

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ABSTRACT

The video driver and extended memory are mounted on two large quad sized PC boards which plug into the LSI-11 Q-Bus. The design incorporates many features to facilitate text editing operations including a linked list, a cursor and the display enhancements. Most of the system parameters are programmable including the CRT controller chip. There are two 128 character generators, one being user programmable RAM. The large display memory can be read or written from the CPU through a memory map register and can function as extended memory to the LSI-11. Typical text displays are 51 lines of 80 characters. In the graphics mode, the displayed field is 512 by 512 pixels. In addition to the CPU port, there is an external port which has access to the display memory, a design feature that can facilitate other uses for the video driver system.

INTRODUCTION

The video driver is part of a "smart" terminal project which will allow users to do text editing and programming off-line from the large time shared computer complex. Virtually every user has a large TV monitor which will now be shared between the network and the local LSI-11 doing text and graphic tasks. A local 300 M byte disk is being brought on-line which will give the users greater independence from the large computers. The LSI-11 system also has a function pad consisting of sixteen lighted keys. This function pad along with the overlay templets gives the operator quick access to the many video driver features that have been built-in.

Specification Highlights - Video Driver

1. Programmable line and character formats.
2. 51 lines of 80 characters, typical alphanumerics.
3. Programmable character font, up to 8 x 16.
4. Two Character Generators (RAM & EPROM).
5. Video enhancements:
   - Blink
   - Reverse
   - Half Intensify
   - Conceal
6. Linked text list.
7. Two mode words per line.
8. Programmable cursor (blinking underline).
9. Display control with Control Status Register (CSR).
10. Mapped memory.
11. Read/Write memory available to CPU.
12. 512 x 512 Bit Graphics (559 Line TV).
13. Graphics Scroll.
14. Interlaced screen.
15. Plugs into LSI-11 bus.

Content

The purpose of this paper is to describe the hardware associated with the video driver and extended memory system. A companion paper is being given on the programming aspects of this equipment.

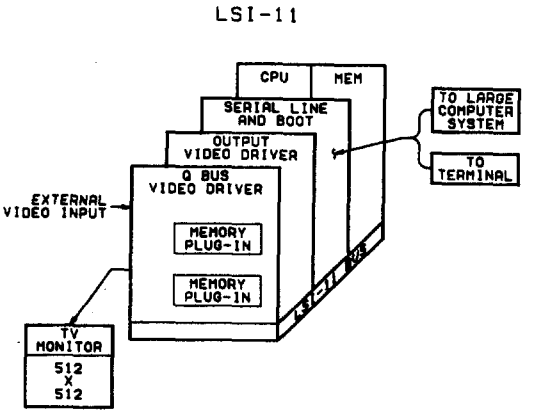

Figure 1: Video Driver with LSI-11

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Video Driver Hardware

The two quad wide PC boards can be divided into ten functional sections. There are more than 200 IC's on these boards which are mostly the TTLS type with several selected Schottky and LSI multifunctional circuits. Due to the system speed requirements, no microprocessor could be used to reduce the chip count. Two standard, dual wide LSI-11 memories become the display memory (DMEM) and plug into special connectors mounted under the first PC mother board. The DMEM bus is compatible with the LSI-11 specifications but is totally separated from the Q-Bus. The video driver hardware effectively takes up three quad card cage slots, and extends slightly beyond the end of the card cage guides.

Interface to LSI-11 Bus

The two quad PC boards plug into the LSI-11 Q-Bus and use the common interface chips designed for the bus impedence and I/O task. The interrupt and DMA signals are not used and there are provisions for soldering bus termination resistor packs should a REV-11 not be present.

Three Port Multiplexer to DMEM

The two memory modules forming the DMEM are connected to what is called an X-BUS. The address and data are multiplexer driven. DMEM access is given to the LSI-11, TV display logic or an external device. The other control signals to DMEM are routed through logic gating and are carefully timed to meet the bus specifications.

DMEM Timing Logic

To achieve proper timing and synchronization of the signals sent over the X-BUS to DMEM, a series of flip-flops driven by a master clock are used. The three requestors, (CPU, TV display logic, external device) all can attempt to access the DMEM but a priority scheme gives preference to the TV first and CPU second. The timing logic is driven by a 96 ns clock that switches the multiplexer from address to data and controls the other X-BUS signals to DMEM. When the memory generates its RPLY signal, another timing sequence is initiated to reset the logic prior to starting the next memory request.

The TV display request data rate must be met or video image distortion will develop. Also, the CPU request to DMEM must be honored within ten microseconds or a bus time out error will be encoured. To accommodate the latter, a 96 ns window is inserted in every fourth TV data request which will allow the CPU to gain access to DMEM before time out. The result is that tight loop CPU requests can distort the TV screen image. In a practical sense, the only time that this is noticed is during a fast block transfer. Complete elimination of this problem could be done if all such transfers were done only during the vertical retrace interval. The vertical sync period is indicated by a bit in the CSR word.

TV Timing Logic

The various timing signals are derived from the 5027 CRT controller which is fully programmable. This controller generates the horizontal and vertical sync, the blanking periods, the scan line number, the row and character count plus several other signals including the cursor control.

Every horizontal sync during the nonblanked portion of the TV image starts a request to DMEM for the header characters and data. The amount of data transferred depends on the display mode and the character scan count, both of which will be discussed later.

The CRT controller clock comes from the 96 ns master clock down counter carry output. Thus, with every sixth or eighth shift, corresponding to a character moved out to the screen, a pulse is sent to the controller to update its character count and internal timers.

Display Data Memory Stack

Transfers of data from DMEM are sent to a fast 16 x 64 Schottky memory which stacks the data until needed by the display. Characters will be sent to the video output while the stack is being loaded from the DMEM which points up the need for the speed to accommodate these overlapping operations. If in alphanumeric mode, the characters that were loaded for the first scan line of a data row will be the same as for the succeeding scans of that data row (typically 5 for interlaced system). Thus, only one access to DMEM is needed for each row, which improves the availability of DMEM to other requestors. The stack accepts sixteen bit words and loads eight bit (character) registers on output.

Dual Character Generators

In alphanumeric mode the ASCII characters coming from the memory stack must be translated into bit patterns which will develop the proper character image on the screen. The character generator does this using the character and scan count as an address input to select the proper pixel pattern for the particular scan line which is loaded into a shift register for serializing. There are two 16 x 128 bit generators, one a fixed ASCII character set and a second user specified in programmable RAM. Each line of text has two mode words, and the active one enables one of the character generators.

Shift Register

Pixel patterns are sent from the character generator to a dual port multiplexer. The other mux input is data coming directly from the memory stack which is used if in graphics mode. The multiplexer output goes to an eight bit shift register that is controlled by the master clock down-counter to conform to the required video data rate, 96 ns per pixel. The resulting pixel pattern is sent to the output conditioning logic.

Output Conditioning Logic

The output from the shift register is conditioned per mode word features selected. Note, no features apply if in graphics. The features are:

Blinking
Concern
Half Intensify
Reverse
Cursor (underline)

The period of the cursor blinking and character blinking are different so one can always be told from the other, no matter what pattern is being displayed.

The active mode word is selected by the most significant bit of the data character. Each mode work can have any combination of video features and choose either character generator set.

Three other output controls are available. Control and status register bits can be set which will reverse the entire screen or stop cursor blinking. Also, there is provision for a light pen option which will make the screen all white while the light pen logic is seeking the picture coordinates.

Register Address Decoding

There are many registers in this system to be programmed and for this purpose addresses 170000-37 have been reserved and decoded. Not all are needed presently, the excess being available to any future external device. Addresses 170000-17 are byte addresses for the 5027 CRT controller chip.

Registers

The list of registers and their functionality follows:

CRT Controller R/W: Twenty byte sized registers that set the video timing and cursor controls.

CSR R/W : Control and status register which is the main control of mode and some system parameters.

Base Address - WO : A pointer to the first word fetched from DMEM for the start of each TV field.

Map - WO : Sets the memory map window size, match address and relocation address.

Format - WO : Determines the scans per character and the data rows per frame.

Link - N.A. : Written by DMEM which loads a pointer to the next line for alphanumerics. Not available to the CPU.

WC & Fill - N.A. : Written by DMEM for the word count and fill character. Alpha numerics only.

Mode Word - N.A. : Written by DMEM. Two eight bit words which control the video output features.

TV DISPLAY SEQUENCE

The video driver produces a subset of the TV standard RS170. We have found this to be totally compatible with our various monitors. Surprisingly, these monitors that were designed for 525 lines per frame will operate at 559 lines without modification. This gives us a viewable 525 by 525 pixel area.

Header Words

TV timing is set by the 5027 controller chip which is continuously generating the sync pulses and blanking period. Any horizontal sync pulse which precede a visual row, will start a header sequence. Three transfers are made from the DMEM to hardware registers as listed above. The first word is a link pointer to the next line, the second word loads the character count and fill character while the third goes to the dual mode words.

Data Push

After the header sequence, the word count register nonzero value will make requests to read the DMEM for input to the 8209 memory stack. This continues until word count goes to zero. The word count is actually the number of eight bit characters and is truly a character count.

Data Pop

Hardware logic controls the memory stack read operation and loads two storage registers as soon as the first word is written to the stack. If no data is written, the fill character is used. The next read occurs only after the first character or its pixel image has been loaded into the shift register. The two eight bit storage registers continue to be loaded in "ping-pong" fashion which gives time for character generator set up. Note that the request to read the stack may be delayed 200 ns if there is a write stack in progress. Thus, the dual eight bit output storage registers are mandatory to assure specified set up times.

Alphanumeric (AN) Mode

The AN mode will use the character generator to develop the character video image. The data MSB sets a flip-flop which in turn enables one of the mode words. The active mode word will then select the character generator, thus two adjacent characters could use different generators, allowing extensive character images. The shifted pixel pattern will be altered according to the selected mode word bits as described above. All three header words are operative. The base address register selects the first AN line from anywhere in DMEM, and the following lines use the link feature.

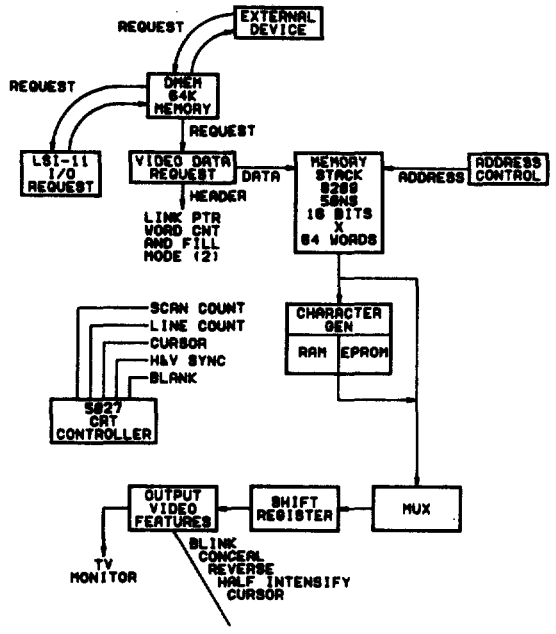

Figure 2: Video Data Flow

Single Field Graphics

With SFG, all three header words are ignored. Instead, the mode words are cleared and the word count is set to thirty-two. Thirty-two sixteen bit words are loaded from DMEM to the memory stack, i.e., 512 pixels for the entire line. This stack data is directly loaded into the shift register.

The base address register asserts the first data word address at the start of the TV field and all succeeding data comes from the progression of this address. Note, the even field must start on an even thirty-two word group since the system is interlaced and the hardware selects odd thirty-two word groups for the odd fields. Note that full screen scrolling both horizontal and vertical can be obtained by manipulation of the base address register.

Output

The data coming from the shift register passes through the output logic and is combined with the sync pulses at the output transistor driver. This driver output goes to the reed relays where the CSR can select one of two video signals for display on the monitor.

DISPLAY MEMORY MAPPING

The two standard LSI-11 compatible dual size memory modules mounted under the mother board hold the data for the video display. There are two ports that can write this memory, the CPU and any external device. The normal use is for data to be generated in the CPU and shipped to DMEM for display. The mapping technique uses a "window" somewhere in the 32K of CPU memory space through which the processor gains access to DMEM.

The Window

The mapping register is at location 170022 and contains three elements:

- Window size
- Match address
- Relocation address

Somewhere in the CPU 32K memory space there must be a disabled memory block. The normal choice is the 4K segment between 24K and 28K although a 2K window from 28K to 30K can be used since BST7 does not disable the DMEM decoder. Thus, the CPU does a read/write operation to the window and a true compare is made with the match address which in turn sets the CPU request flip-flop. The CPU address is saved in a video board register and waits until the CPU request is honored. When the CPU is granted the request, the high order address bits come from the relocation register which effectively move the window about the DMEM space. Care must be taken with the boundary conditions for when writing across a window boundary, the relocation register must be updated or else the data wrap around and rewrite the window again.

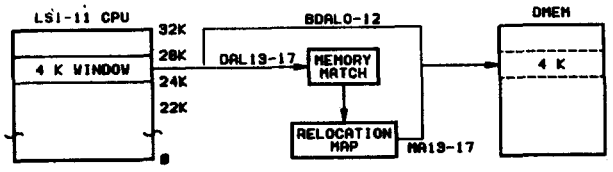

Figure 3: Memory Mapping

Relocation

The relocation register has eighteen bits of addressing which will be adequate for the expected 128K memories. The CSR has two bank select bits to enable one of the two DMEM modules and provide an eventual 256K words of display memory.

The RPLY signal from DMEM along with the data transfer are sent to the CPU Q-BUS within the ten microsecond bus time out period.

OTHER POINTS

Light Pen

A light pen option has been provided for by allowing an external device to "flash" the screen, i.e., for light pen sensing. Virtually all the

timing and synchronization are available on the board to run X and Y axis counters in a light pen interface. Such an interface could be a counter circuit with output to a DRV-11 parallel interface card for transferring light pen coordinate information to the CPU.

External Port

This port to the display memory could be used to load large blocks of data coming from some other device. The X-BUS signals are available on the back edge connector, so such an operation could be transparent to the CPU.

TV Screen Overlay

A technique for overlaying a TV image with an image from the DMEM is being designed. Thus, a cursor type operation can be obtained where the DMEM would generate a cursor image that could be scrolled around on the TV screen. The coordinates would be known to the LSI-11. The function pad mentioned earlier is programmed to facilitate cursor movement.

Refresh DMEM

The older LSI-11 MOS memories required external refresh and the video board has that capability as a strappable option. However, that option is usually disabled as all present memories have onboard refresh and are entirely compatible with the video memory requirements. They all use the distributed refresh technique, taking 400 ns periods every few microseconds.

Partial Color

The mode word has unused bits which could be implemented to designate limited alpha numerics color. Only two colors per row would be available, and two more output driver stages would have to be built and gated. The output would be three RS 170 type (RBG) signals which would require a compatible monitor.

Half Shift Right

Half shift right logic is included in the hardware but we found that it is not needed with the normal 6 x 10 character font. The typical character viewable image is five by seven dots and is very clear. Half shift feature if of more value on larger character fonts where edges need to show more rounding.

ACKNOWLEDGMENTS

During the design phase of this project, we received many inputs from a large group of well-qualified people, which were very valuable in developing a user oriented product. I am particularly appreciative of Jerry Owens, the project leader and John Fletcher and Bob Judd of the Computations Department.